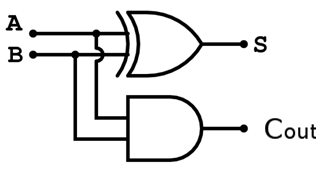
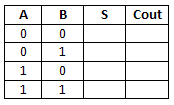
Combination of Logic Gate

**Question 1:** Half-Adder

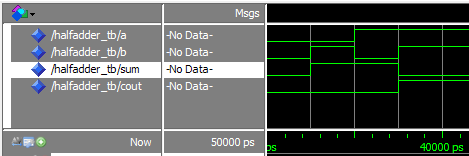
****

**Figure:** Half-Adder circuit

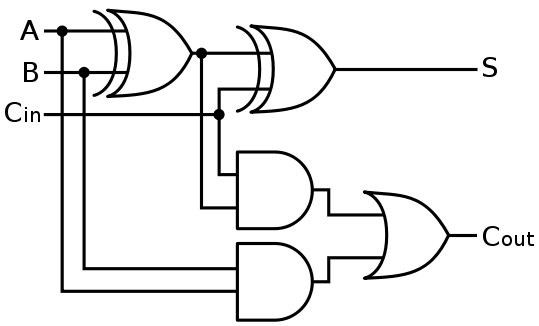
Above is a detail diagram of the half-adder circuit. It consists of one two-input AND gate and one two-input XOR gate. Fill the truth table output based on the circuit given and write VHDL code for Half-Adder followed by constant 50ns testbench. Your waveform should look like the result below.



**Result:**

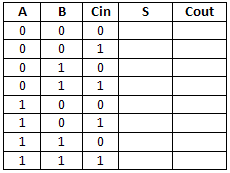


**Question 2:** Full-Adder

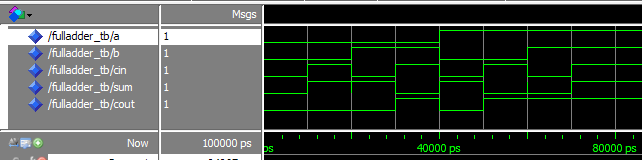
****

**Figure:** Full-Adder circuit

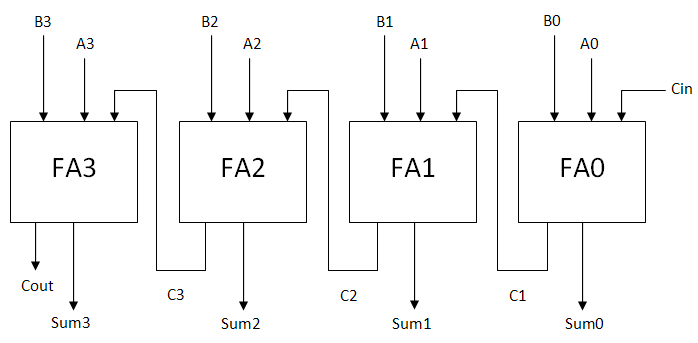
Above is a detail diagram of the Full-adder circuit. It consists of two two-input AND gates, two two-input XOR gates and one two-input OR gate. Fill the truth table output based on the circuit given and write VHDL code for the Full-Adder followed by constant 80ns testbench. Your waveform should look like the result below.

****

**Result:**

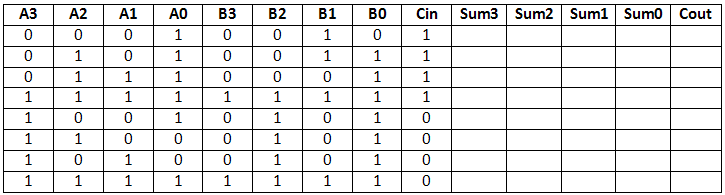


**Question 3:** 4-bits Full-Adder

****

**Figure:** 4-bit FullAdder circuit

Above is a diagram of the 4-bit Full-adder circuit. It consists of 4 full-adder modules which are connected with each other. Based on the information given, write VHDL code for the 4-bit Full-Adder design. Then, use your 4-bit full-adder waveform result to complete the truth table below.



**Result:**

